IN THE SPECIFICATION:

Please **amend the paragraph beginning on page 1, line 7,** as follows:

It is known to use an analogue chip to recover, in digital format, analogue data which is recorded on a medium, such as a tape. Referring to Figure 1 of the drawings, which illustrates a simplified version of such analogue chip, such a data recovery circuit generally comprises a variable gain amplifier (VGA) 100, which receives analogue ~~data~~ signal 102 from a tape (not shown), a filter 104 to smooth the analogue ~~wave form, and~~ waveform, an analogue-to-digital converter (ADC) 106 for converting the smoothed analogue waveform 108 into a 6-bit digital signal, a digital signal processing module 110, a Viterbi ~~detector~~ decoder 112 to produce a 6-bit output, and an RRL decoder 114, which produces 4-bit output data.

Please ~~amend~~ **the paragraph beginning on page 1, line 27,** and **ending on page 2, line 12,** as follows:

When analogue data is read from a tape (not shown), it is common for errors to occur, which result in bad data being read. For example, the tape may flap away from the tape head ("drop-out") or the temperature of a magneto resistive head may suddenly change, causing a thermal asperity. A change in the head temperature causes a change in the head resistance resulting in a DC shift in the analogue signal. The temperature

of the head can change suddenly when a piece of dust or debris on the tape hits the head. The dust or debris either heats the head due to friction, or cools the head by conduction. The tape channel is AC coupled to the head so, after a certain amount of time (dependent upon the magnitude of the DC shift), the signal comes back into range. However, in the meantime, the DC shift can cause the timing lock of the clock 116, which controls the sampling time of the analogue-to-digital converter 106, to be lost. To prevent or rectify this problem, the conventional circuit includes a thermal asperity detector 118, the output of which is fed to the digital signal processing module 110, which controls the timing recovery circuit 120. Asperity detector 118 thus detects an event that alters or destroys analogue input signal 102.

Please **amend the paragraph beginning on page 2, line 19,** as follows:

In the conventional circuit, however, the output from the digital signal processing module 110 is still fed to the Viterbi ~~detector~~ decoder 112 which outputs the most likely sequence of data to be input to the RLL decoder 114. ~~Detector~~ Decoder 112 does not known that the data it is processing is bad data and outputs a sequence of data to the RLL decoder 114 in the usual manner. Not every sequence of bits is a valid RLL encoded sequence, and the RLL decoder 114 marks such invalid sequences

as errors by setting an erasure flag to 1. The erasure flag is 0 if the sequence is a valid RLL encoded sequence.

Please **amend the paragraph beginning on page 2, line 27**, as follows:

In the prior art circuit, though, some of the data sequences output by the Viterbi ~~detector~~ decoder 112 in response to bad data are valid RLL encoded sequences (even though they are incorrect) and, as such, are not recognised as errors so no erasure flag is set. Nevertheless, as stated above, it is highly desirable for the error correction circuit (not shown) to know the location of errors, as this doubles its error correction capability.

Please **amend the paragraph beginning on page 6, line 19**, as follows:

In Fig. 2, however, the thermal asperity detector 118 is also connected to the Viterbi ~~detector~~ decoder 112 via a shift register or delay circuit 122. The thermal asperity detector 118 holds positive and negative thresholds and operates in accordance with an algorithm which states that if the analogue waveform read from the tape exceeds the positive or drops below the negative threshold for more than a predetermined period of time, then thermal asperity has occurred. Thus, if the analogue waveform 102 exceeds the positive threshold or drops below the negative threshold for more than the predetermined

time period, thermal asperity detector 118 derives an output signal indicating detection of an event that causes altering or destroying of analogue signal 102. The thermal asperity detector 118 sends one or more event signals to the Viterbi ~~detector~~ decoder 112 indicating that thermal asperity has occurred and continues to send such event signals until the thermal asperity ends, i.e. the input signal returns to a value within the threshold(s).

Please **amend the paragraph beginning on page 7, line 1,** as follows:

Viterbi ~~detector~~ decoder 112 responds to receipt of the signal from the thermal asperity detector 118 to produce invalid RLL encoded data sequences for the duration of the bad data caused by thermal asperity, thereby causing the RLL decoder 114 to produce erasures for each sequence resulting from the bad data.

Please **amend the paragraph beginning on page 7, line 7,** as follows:

Of course, the output of the shift register 122 could be connected directly to the RLL decoder 114, thereby causing the RLL decoder to set the erasure flags for each sequence of data resulting from the bad data. However, this is only really practical if the RLL decoder 114 is on the same chip as the

thermal asperity detector, which it often is. Otherwise, additional pins and connections would be necessary.